# *A Novel Bipolar XOR/XNOR Realization using Translinear Type 2nd Generation Current Controlled Current Conveyor Designed in 45nm CMOS Technology*

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***Abstract:*** *The current controlled current conveyor (CCC) has emerged as a reasonable design device for analog electronics, and has proved to be a design building block ensuring low voltage and low power solution as per the requirements of present day VLSI. Second generations CCC's (CCCII) are found more flexible as the circuit design is concerned. A survey of the literature published so far shows the utility of the device in analog applications only. However, this device is found equally suitable for digital applications as well. Therefore, a few of the basic digital applications are investigated here to validate the new hypothesis. The applications studied here are restricted to one and two input variables only and single stage circuits.*

**Keywords:** CCCII circuit applications, CCCII based digital building blocks, CCCII based digital circuits, Current mode digital applications, CCCII based XOR/XNOR realization.

## 1. INTRODUCTION

Recently, the CCCII has become popular in implementing both voltage-mode (VM) and current-mode (CM) signal processing circuits. Since these devices offer high performance and are highly versatile, therefore a variety of applications can be seen in the constantly pouring in literature in various technical publications, [1-8]. Researchers are trying to utilize CC's in Circuits, Systems, Communication, Measurements, Analog FPGA etc [9, 10]. System design is inclined towards mixed signals. Two level logic is felt deficient. Multiple valued logic is expected to reduce complexity of the digital systems [11]. Basically the CCCII is an analog device. It's characteristic analytical model is presented here in Eq.1 and the block diagram is given in Fig 1.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

Here, X is the low impedance input node, Y is high impedance input node and Z is high impedance output node, $V_X$, $V_Y$, $I_X$, $I_Y$ and $I_Z$ are voltages and currents of the nodes X and Y and Z respectively, $I_B$ is the biasing current. The ± sign in Eq.1 represents the type of the CCCII. For CCCII+, the currents $I_X$ and $I_Z$ flow into or out of the device simultaneously. For CCCII-, the direction of $I_X$ or $I_Z$ is reversed as to what is assumed for CCCII+. A CCCII can offer multiple $\pm I_Z$.

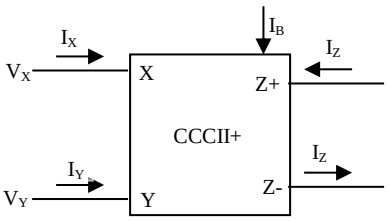


**Fig. 1.** Block diagram representation of a CCCII+.

It has been observed that the CCCII can also be applied to the design and implementation of various digital applications. A few digital applications are reported in [8,12]. These applications are realized by using CMOS CCCII.

In the present work XOR nature of the CCCII is investigated and the realization for XOR/XNOR is proposed. These propositions are simulated on Hspice using the standard high performance 45nm CMOS parameters [5].

## 2. THE XOR FUNCTION

XOR is an important digital function and has realizations in all circuit methodologies. The usual symbol is presented in Fig.2 (a) and the basic transfer characteristics of the function are presented in Table 1. The output is unipolar in nature. Bipolar logic realization is pointed out and suggested useful in multilevel logic realization [13]. The symbol of the

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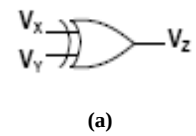
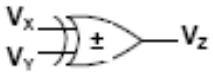
bipolar XOR is presented in Fig.2 (b) and the corresponding transfer characteristic is presented in Table2. The output exhibits both (+) and (–) signal polarities with respect to ground. In Table 2, the polarity of the output signal is different for ($01_2$) and ($10_2$) inputs. ($01_2$) etc. represents binary numbers.




(a)

**TABLE 1**
Unipolar XOR Characteristic

| $V_X$ | $V_Y$ | $V_Z$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |




(b)

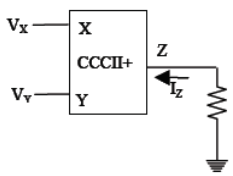
**TABLE 2**
Bipolar XOR characteristic

| $V_X$ | $V_Y$ | $V_Z$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | $\pm 1$ |
| 1 | 0 | $\mp 1$ |
| 1 | 1 | 0 |

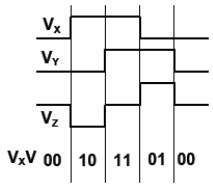
**Fig. 2.** XOR functional symbols and their truth tables: **(a)** Unipolar XOR; **(b)** Bipolar XOR.

## 3. XOR NATURE OF THE CCCII

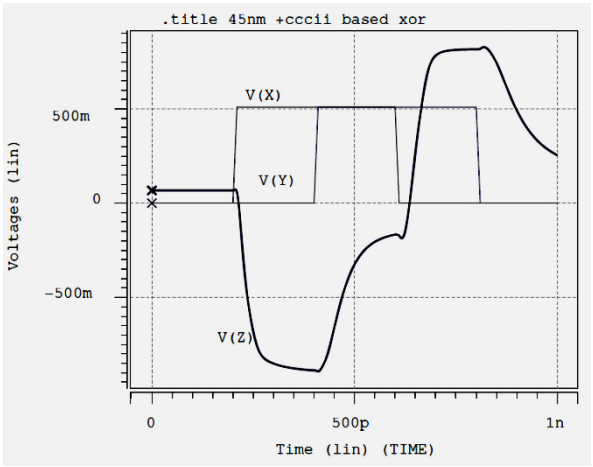
It is observed that the CCCII naturally exhibits The CCCII+ circuit is shown in Fig.3. Voltage pulse inputs applied are applied to it's X and Y nodes. The analysis is done as per the following logic combinations




(a)




(b)




(c)

**Fig. 3. (a)** XOR characteristic of the CCCII; **(b)** Bipolar representation of the XOR truth table; **(c)** Simulation results.

[14]

a. **$00_2$** or **$11_2$**

$$V_X = V_Y = 0 \text{ or } V_X = V_Y = V,\ I_Z = 0; \quad (2)$$

b. **$10_2$**

$$V_X = V,\ V_Y = 0,\ I_Z = \frac{V}{R_X}; \quad (3)$$

c. **$01_2$**

$$V_X = 0,\ V_Y = V,\ I_Z = \frac{-V}{R_X}; \quad (4)$$

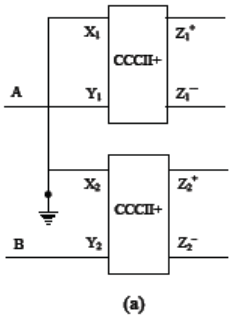
Same results as proposed in Eq.2, 3 and 4 are obtained by simulation of the circuit of Fig.3 (b). Clearly, Fig.3 (b-c) corresponds to the bipolar XOR function and the current in the output resistor attains a three level logic.

**TABLE 3**
Performance Details of the XOR of Fig.3(a)

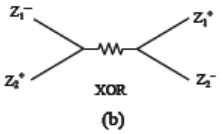
| | |
|---|---|
| Delay | ≈ 30ps |
| Average Power | ≈ 64μW |
| Biasing | = ±1V |
| Peak Current | ≈ ±13μA |
| Offset Current | ≈ 50.0nA (**$00_2$**) |
| | ≈ 3μA (**$11_2$**) |
| NMOS | 0.1μm/0.1μm |
| PMOS | 0.3μm/0.1μm |
| $R_Z$ | 50K (optional) |

## 4. CCCII BASED XOR REALIZATION SCHEMES

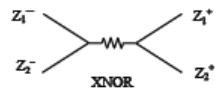
A general scheme for XOR/XNOR realization is proposed in Fig.4. Two identical CCCII's of $I_{Z+}$ and $I_{Z-}$ are used. An XOR circuit working with $V_A$ and $V_B$ signals can be developed by using Fig.4 (a–b).




(a)




(b)




(c)

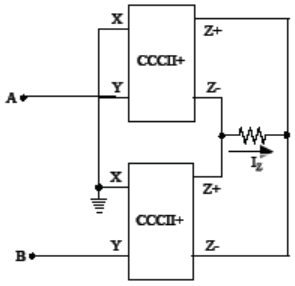
**Fig. 4.** XOR/XNOR Realization topologies; **(a)** the logic driving circuit; **(b)** and **(c)** are sensing circuits for the XOR/XNOR functions respectively.

In this case, $X_1 = X_2 = 0$. Logic HIGH/LOW = ±V, the output drive $I_{Z+}$ is calculated using Eq. 2–4. It is observed that the output drive is doubled due to the additive effect at the nodes joining $Z_{1+}$, $Z_{2-}$ and $Z_{1-}$, $Z_{2+}$ and enhances the operation speed.

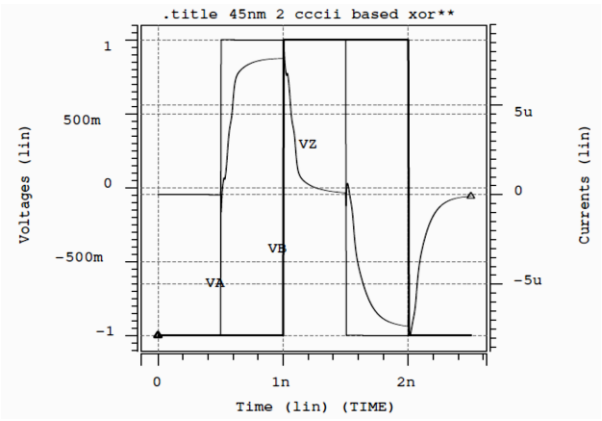
The proposed circuit for XOR realization is shown in Fig.5 (a) and it's Truth Table is given in table 4. Fig.5(b) shows the simulation results of Fig. 5(a).

**TABLE 4** :
Functional Details of XOR Realization of Fig. 8. Here, LOGIC '1' = $V_{DD}$ = V; LOGIC '0' = –V; I=V/$R_X$

| A | B | $I_Z$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 2I |
| 1 | 0 | –2I |
| 1 | 1 | 0 |




**(a)**



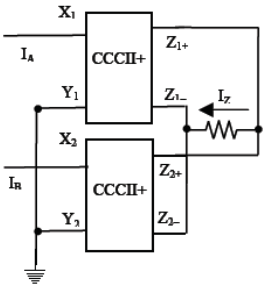

**(b)**

**Fig. 5. (a)** XOR realization Topology for voltage inputs; **(b)** output current signal for input voltage combination as per Table 3.

**TABLE 5**
Performance details of the proposed XOR in Fig.4(a)

| | |
|---|---|
| Delay | ≈ 60ps |
| Average Power (62µW per CCCII) | ≈ 124µW |
| Biasing | = ±1V |
| Peak Current | ≈ ±8µA |
| Offset Current | ≈ 0.0µA |
| N/PMOS : | 0.1µm/0.1µm |

XNOR function can also be similarly realized by connecting output nodes of Fig.4 (a) with Fig.4(c). Current signals inputs can also be used. A possible XNOR realization is shown in Fig.6 (a). Current inputs $I_A$ and $I_B$ are applied to the low impedance input nodes. Output current is presented in Fig 6(b), and the circuit details and performance are summarized in table 7.




(a)

**TABLE 6**
Functional details of current input XNOR Circuit

| $I_A$ | $I_B$ | $I_Z$ |
|---|---|---|
| –I | –I | 2I |
| –I | I | 0 |
| I | –I | 0 |
| I | I | –2I |

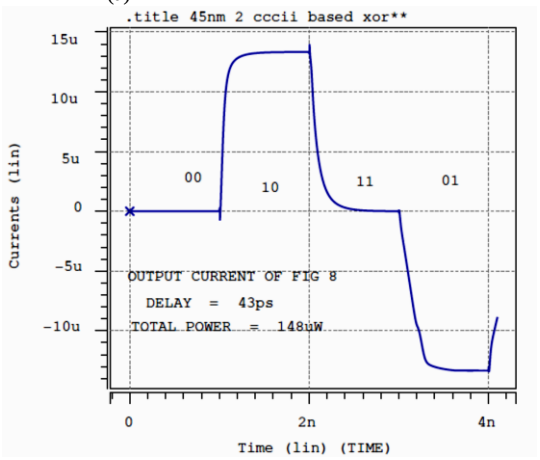



**Fig. 6.(a)** Current input XNOR realization; **(b)** output current of the XNOR.

**TABLE 7**
Performance details of the proposed XNOR of Fig.6(a)

| | |
|---|---|
| Delay | ≈ 43ps (for +half) |
| Average Power (74µW per CCCII) | ≈ 148µW |
| Biasing | = ±1V |
| Peak $I_Z$ Current | ≈ ±13µA |
| Offset Current | ≈ 0nA (**00**$_2$)<br>≈ 6nA (**11**$_2$) |
| N/PMOS : | 0.1µm/0.1µm |
| Technology | 45nm CMOS |

## 5. MINIMUM MEASURABLE PHASE DIFFERENCE IN INPUT SIGNALS

The minimum phase difference these circuits can differentiate depends their delay characteristics. For 50% mark as reference, the input signal time difference should be larger than delay.

$$t_{\Delta\varphi} > t_{DELAY} \qquad (5)$$

For CCCII based XOR realization it is estimated that the delay ≈ 50ps. Therefore the phase difference of the input signals should be larger than a corresponding phase equivalent to 50ps. This timing restriction causes measurement errors if the signal frequency is above megahertz range, as the time period $T$ becomes comparable with the $t_{DELAY}$. In the present case, if the

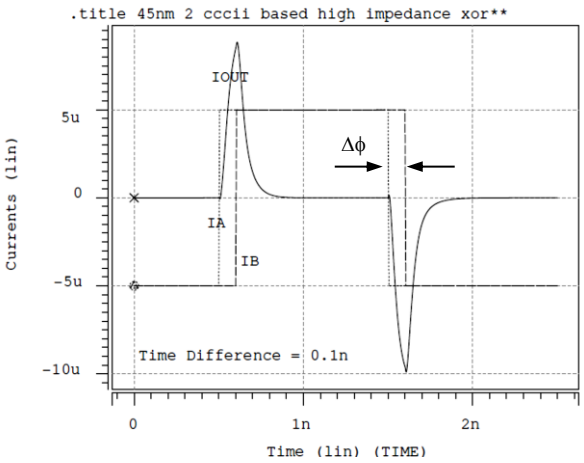



**Fig. 7.** Measurement capability of the proposed CCCII XOR. $I_B$ is delayed by 0.1ns with respect to $I_A$. Both $I_A$ and $I_B$ are 2ns pulses. 0.1ns delay corresponds to 18° phase difference.

XOR operates at 1GHz frequency, the phase difference error is ~0.533% for a system operating at 1GHz clock.

## 6. SIMULATION RESULTS AND VERIFICATION

In this work, bipolar XOR/XNOR realizations using the popular CCCII are proposed. For the purpose of verification, results are obtained by using Hspice. The CMOS model cards are Beta Version PTM 45nm High Performance parameters [15]. The results are presented in Figs.3(c), 5(b) and 6(b). The CCCII used in this work is adapted from [5], keeping in view the nature of the circuit functions, the sizes of the transistors were optimized to achieve the total average power low. The results obtained confirm the underlying principles. Efforts are hereby successfully made to extend the utility of a CCCII to the digital applications.

## 7. CONCLUSION

This effort brings out the fact that the popular CCCII can also be a preferable device for digital applications. In the forgone propositions, investigations are carried out to exploit the basic nature of a CCCII, voltage difference to current conversion and the current conveyance, to realize XOR/XNOR functions.

Parasitic resistance of the CCC establishes current in the circuit. But generally, an exact value bears no significance, therefore this resistance need not be calculated accurately. The CCC used here was designed for analog applications, 74μW/CCC power is required. Translinear type is a good design choice as it attains very high bandwidths, 350MegaHz.

## REFERENCES

1. M.T. Abuelma'atti and M. A. Al-Qahtani, \On the realization of the current controlled currentmode amplifier using the current controlled conveyor," International Journal of Electronics, vol. 86, pp. 1333-1340, 1999.
2. S. Maheshwari, \High CMRR wide bandwidth instrumentation amplifier using current controlled conveyors," International Journal of Electronics, vol. 89, pp. 889-896, 2002.
3. S. Maheshwari and I.A. Khan, \Simple first-order translinear-C current-mode all-pass section," International Journal of Electronics, vol. 90, pp. 79-85, 2003.
4. S. Maheshwari, \New voltage and current-mode APS using current controlled conveyor," International Journal of Electronics, vol. 91, pp. 735-743, 2005.
5. M.Y. Yasin, B. Gopal,"High frequency oscillator design using a single 45nm CMOS current controlled current conveyor (CCCII+) with minimum passive components", International journal of circuits and systems, vol.2, issue 2, April 2011, pp. 53-59
6. Chuachai Netbut, Montree Kumngern,Pipat Prommee, and Kobchai Dejhan,New simple square-rooting circuits based on translinear current conveyors", ECTI Transactions on Electrical Engineering, Electronics and Communications, vol.5, issue 1 February 2007, pp.10-17.
7. Jiun-Wei Horng, Chun-Li Hou, Chun-Ming Chang, Hao Yang, Woei-Tzer Shyu, "Higher-order immittance functions using current conveyors", Mixed signal letters, Analog Integr Circ Sig Process (2009) 61:205–209
8. Firdaus Majeed, "Low Voltage Low Power Design of CCCII in 45nm CMOS Technology and it's applications to Analog and Digital Circuits", M.Tech. Thesis submitted at Integral University, Lucknow, Uttar Pradesh, India, May 2011.
9. V. Stopjaková and H. Manhaeve, CCII+ Current Conveyor Based BIC Monitor for IDDQ Testing of Complex CMOS Circuits, EDTC '97: Proceedings of the 1997 European conference on Design and Test, IEEE Computer Society, March 1997, p 266-270.
10. Christophe Premont, Richard Grisel, Nacer Abouchi, Jean-Pierre Chante, A Current Conveyor based Field Programmable Analog Array, **Analog Integrated Circuits and Signal Processing,** Volume 17 Issue 1-2, September 1998, Springer.
11. Akira Mochizuki, Takahiro Hanyu, Low Power Multiple Valued Current Mode Logic using Substrate Bias Control, IEICE Trans., Electron, Vol. E87-C, No.4, April 2004. p 582-588.
12. Firdaus Majeed and M.Y. Yasin, A Novel Voltage Comparator and it's Application – A New Simple Configuration Based on 45nm 2nd Generation Current Controlled Current Conveyor, Acta Electrotechnica, volume 53, Number 2, 2012, pp 112-114.
13. Wasim Ahmad, "Biphase amplifier for precision controlled rectification and polar logic operation", IEEE Transaction on Industrial Electronics, vol. 38, no.1, February 1991.
14. Low-Voltage Low-Power Cmos Current Conveyors, Giuseppe Ferri, Nicola C. Guerrini, Kluwer Academic Publishers, New York, 2003.
15. High Performance PTM 45nm CMOS parameters, 2006. http://ptm.asu.edu.

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