Practical implementation of a half-bridge SRM converter for low power applications

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Abstract *– The paper is presenting the practical implementation of a half-bridge converter driving a switched reluctance motor. One of the advantages of the proposed converter topology is that it ensures independent control for each motor phase. The measurements are concentrated on two motor types, namely a four phase SRM and on a two phase, high-speed SRM. The main objective of the paper is the working principle demonstration and to point out the main advantages/disadvantages of the proposed topology and emphasize future developments.*

Keywords –*Half-bridge, SRM, bipolar drive, capacitor, high speed*

1. INTRODUCTION

The requirements from the customer side are continuously becoming more stringent both in terms of performance as well as the cost. Meeting the performance requirements in the given conditions is mandatory for an electric drive motor, but very often its final cost based on which one chooses between different available options. Therefore the continuous struggle for improving the performance characteristics of the PM-less of PM-free machines [1]. Due to well-known issues, discussions and limits (i.e. lower efficiency and power density when compared to rare earth-based PMSMs, high torque ripple and NVH) [2], for specific applications SRM can be a part of the solution.

The most used topology for switched reluctance machine is asymmetric bridge topology which is a two quadrant DC-DC converter [3], operating under unipolar current condition. It is generally known that this converter topology provides the biggest number of advantages and the smallest number of disadvantages when driving a SRM [4]. However, the biggest drawback of the asymmetric bridge topology is represented by the fact that such a topology contains two diodes and two transistors per one phase, which means a higher cost when compared with conventional converters for PMSM, wherein only two transistors per phase are used. One further aspect from the semiconductors point of view is that there are not many standardized power modules on the market having an asymmetric bridge configuration (2 transistors and 2 diodes) compared to regular half bridge configuration. Therefore the usage of discrete components for asymmetric bridge is necessary. Furthermore, special care has to be paid when calculating the ratings of the additional power diodes as due to high internal resistance the losses may exceed very fast the value corresponding to stable thermal behavior, thus either larger diodes or expensive cooling is needed. The most of available MOSFET and IGBT transistors are manufactured with a build in anti-parallel diode, a fact that cannot be exploited in a cost effective way for SRM motor drive.

The switched reluctance machine can operate under bipolar excitation regime, since the torque is not dependent upon the direction of the current, therefore the possibility of using the conventional voltage source inverter (VSI) to drive an SRM have been exploited in [5-7], however with a big drawback considering the fact that the use of Y-connection of the motor windings is increasing the magnetic coupling between the motor phases thus, eliminating the independent phase control capability. In [8] attempts have been made to drive a 3 phase machine by means of a 3 phase VSI used in conjunction with a regular half-bridge topology. Bipolar current excitation has been applied to the motor phases but the motor cannot handle a full independent current control and the overlapping condition between phases can be difficult. In this work, a method for eliminating this drawbacks is proposed and validated by measurements on two types of SRMs having different range of working speeds.

The work is structured in four sections as follows. In Section II, the considered topology is studied and the operating principle is explained by showing the current paths modes and conducting switches. In section III the practical implementation and the measurements are done for two SRM topologies. Finally the conclusions are drawn in the last section.

2. CONVERTER TOPOLOGY DESCRIPTION

The considered converter topology based on regular half bridge configuration for driving an SRM was at first introduced in [9]. It promises independent phase control and is made by using commonly found transistor and diode in a chip, which is the state-of-the-art technique in half bridge converter topologies, such as VSI used for driving 3 phase PMSM.

A single phase representation of the half bridge converter topology driving the SRM is shown in Fig. 1. In Fig. 2 the converter is illustrated for a three phase machine but it can be straightforwardly extended for any number of phases needed.

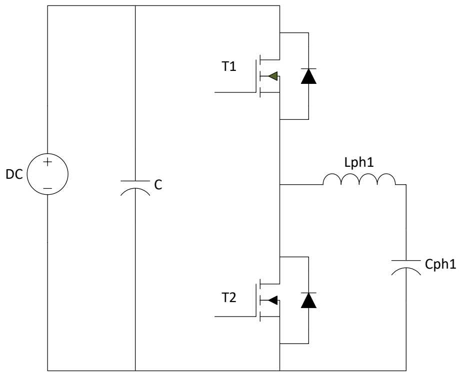


Fig. 1. One phase representation of the considered converter

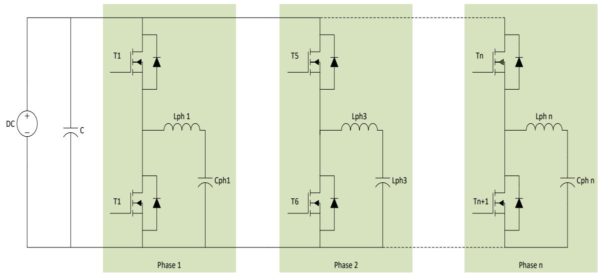


Fig. 2 Extention of the proposed topology for a three phase SRM

The operating modes possible (Fig. 4a, Fig. 4b, Fig. 5a, Fig. 5b) for such a converter topology can be explained according to the presumptive timing waveforms (depicted in Fig 3) over the time intervals t_k as follows:

- Time intervals, are defined as t_{2k+1} with $k = (0,1,..4)$, in which the phase fluxing is accomplished by turning ON the high side transistor, whereas the low side transistor is kept in OFF state. Over these time periods, the capacitor connected in series with the phase is charging from the DC bus power rail. For this mode of operation (positive cycle fluxing), the current circulation path is shown in Fig. 4a.
- During the time intervals defined as t_{2k+2} with $k = (0,1,..4)$, the high side transistor (T1) is put in the OFF state, forcing the phase to be de-fluxed through the anti-parallel diode from the transistor T2 which became forwarded biased. At the beginning of the positive cycle period, the capacitor having low amount of energy stored, the de-fluxing current have a lower slope of

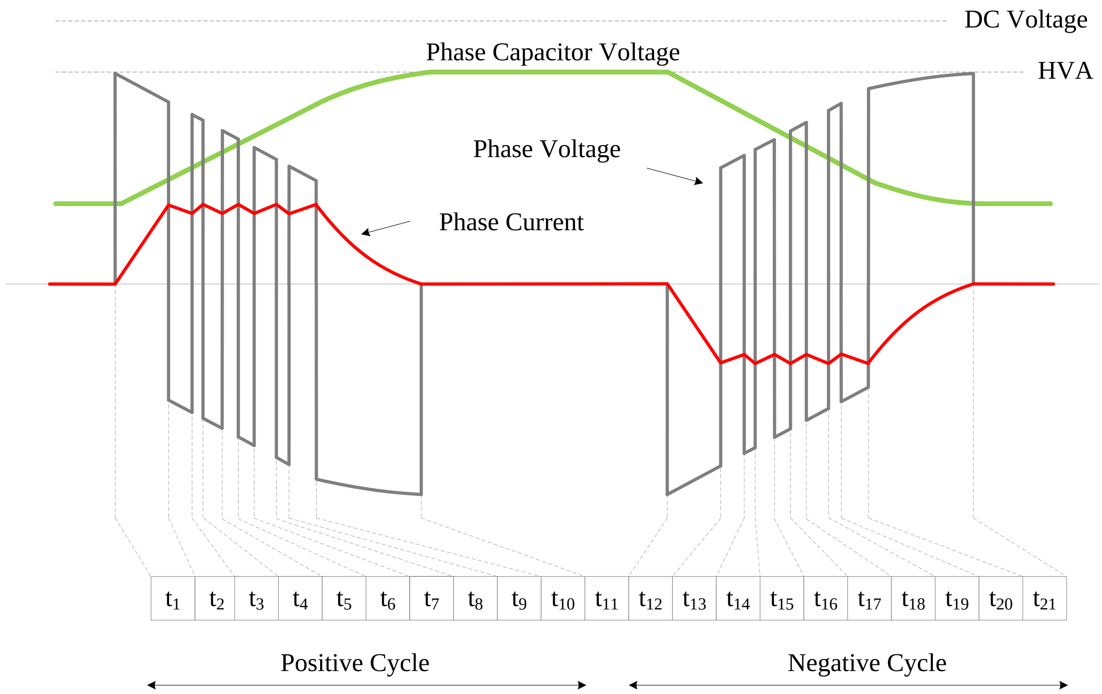


Fig. 3 Presumtive waveforms for a SRM phase

descending as well. When the voltage level across the capacitor has an increased value, the slope of the de-fluxing current is increasing. The capacitor charges during the de-fluxing period. The converter current circulation path for this operating mode of is shown in Fig. 4b.

- During the time intervals defined as t_{11}, the both transistors are in the OFF state and there is no current flow in the motor phase. The voltage across the capacitor during this period of time reaches its maximum value.
- During the time intervals defined as t_{2k+2} with $k = (4,5,..8)$,the phase fluxing is accomplished by switching ON the low side transistor, while the transistor from the upper side is kept OFF. The current in the machine phase during this operating mode have negative values its circulation path being shown in the Fig. 5a.
- During the time intervals defined as t_{2k+1} with $k = (6,7,..10)$, the low side transistor (T1) is put in the OFF state, forcing the phase to be de-fluxed through the anti-parallel diode of the transistor T1. At the beginning of the negative cycle period, the capacitor has the maximum stored energy; the de-fluxing current of the phase is made with a lower slope. When the voltage level across the capacitor has an increased value, the slope of the de-fluxing current is higher. The current path for this operating mode converter is presented in Fig. 5b.

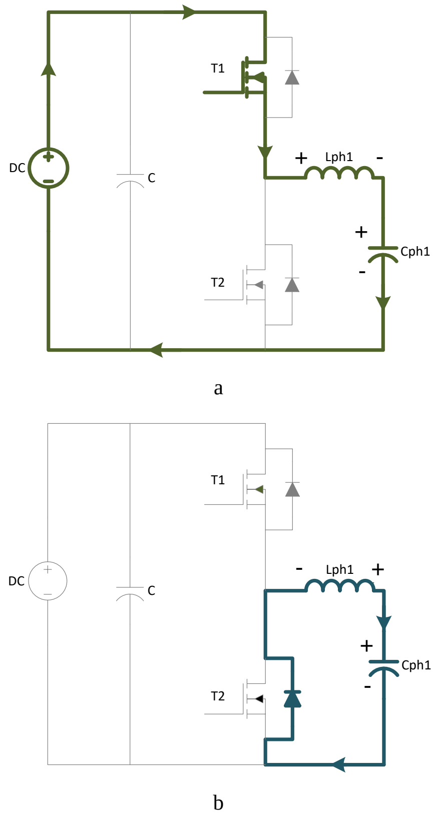


Fig. 4. Working principles. a) Positive cycle fluxing b) Positive cycle de-fluxing

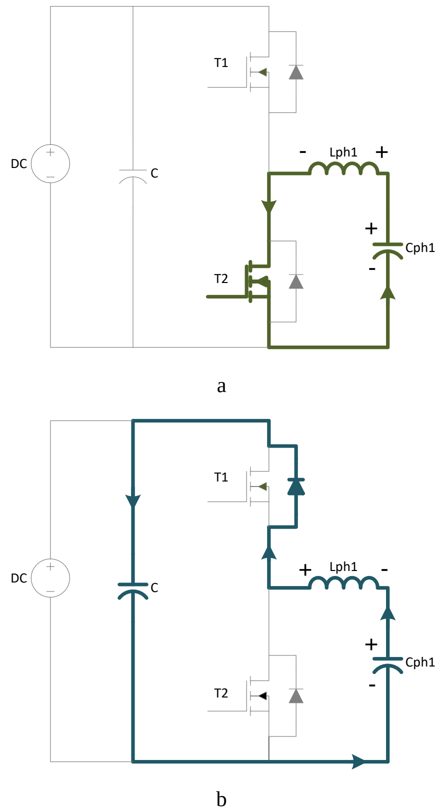


Fig. 5. Working principles. a) Negative cycle fluxing; b) Negative cycle de-fluxing

3. EXPERIMENTAL RESULTS OF THE HALF BRIDGE BASED SRM CONVERTER

The proposed converter topology has been experimentally tested on two different commercially available switched reluctance machines. Firstly, tests have been conducted on a four phase machine having a number of 8 stator poles and 6 rotor poles 8/6 SRM. In the second part, the experimental measurements have been made on a commercially available high speed two-phase 4/2 SRM.

After developing the required models in Simulink they were compiled in order to be loaded on the dSPACE-based rapid-control prototyping platform.

In Fig. 6 one can see the phase currents when the 8/6 SRM is supplied with bipolar current. The reference current for the test below is set to 1.2A and a hysteresis band of 0.25A is employed, whereas the speed of the motor is set to a low value of 300 rpm. Fig.7. presents the acquired data (using an oscilloscope) of some of the signals on the converter with respect to one phase. Channel 1 is showing the phase current (phase 1), while Channel 2 shows the phase capacitor voltage. On Channel 3, the upper transistor drain-source voltage is displayed, whereas the phase voltage is shown on channel 4.

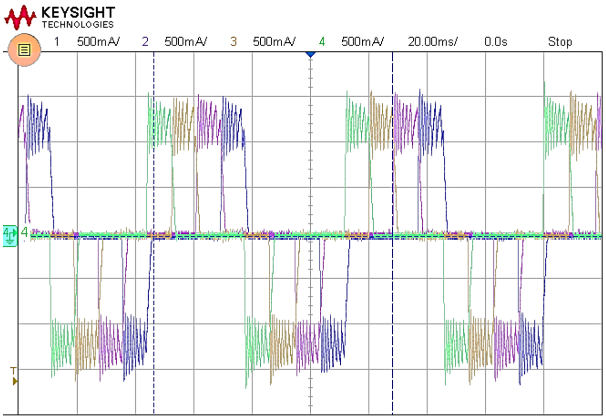


Fig. 6 Experimental results of the half bridge based converter Bipolar phase currents applied to an 8/6 SRM

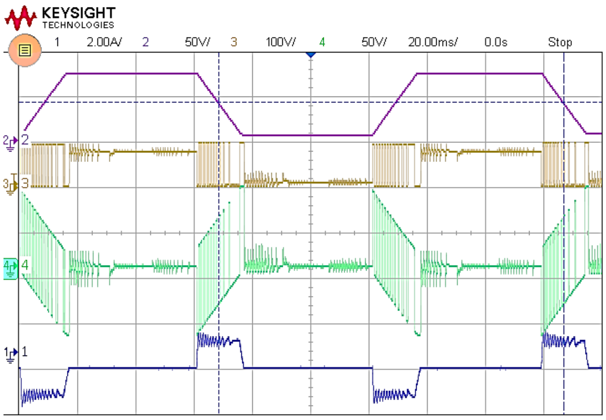


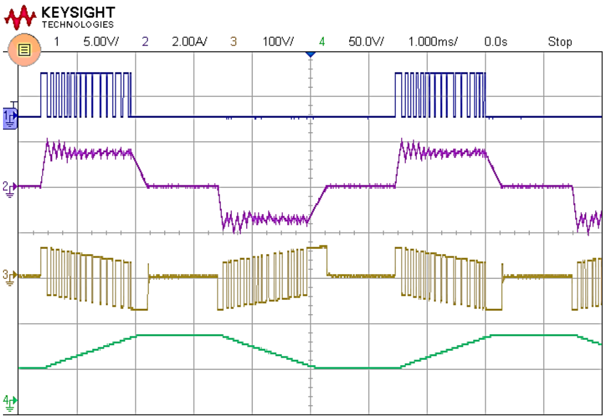
Fig. 7. Experimental results of the half bridge based converter Phase current and voltage, control signals applied to an 8/6 SRM

The same tests have been successfully done, considering this time a high speed switched reluctance machine (4/2 configuration stator poles over rotor poles), running at 12 000 rpm. The objective was to verify and to assess the behaviour of the proposed half bridge based converter topology on such operating conditions. The simulated model was developed and adapted to this specific two phase machine, and afterwards real time implementation has been done. Some of the results acquired by means of an oscilloscope are shown in Fig 8 and Fig 9.

In the waveforms depicted in Fig 8a, one can observe on channel 1 the control signals applied to the gate of the transistor from the upper leg of the half bridge. On channel 2 and channel 3 the phase current and phase voltage have been displayed. Finally on channel 4 on the graph the capacitor voltage is shown.

Similarly, tests have been conducted at higher speeds, and the obtained results are shown in Fig. 8b, Fig. 8c, Fig. 8d.

In the Fig 9, the two phase currents are shown on channels 1 and 2. On the channel 3 the phase voltage associated to the phase 1 is highlighted, whereas on the



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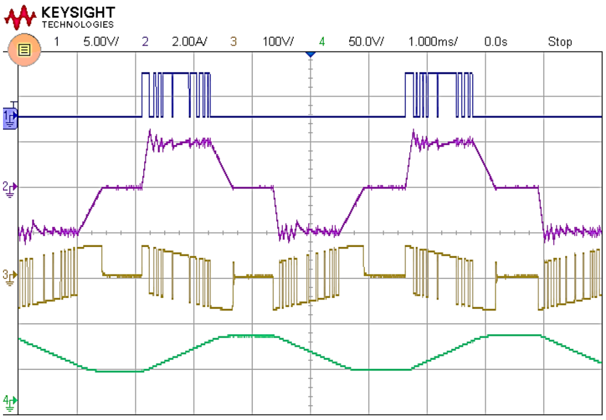

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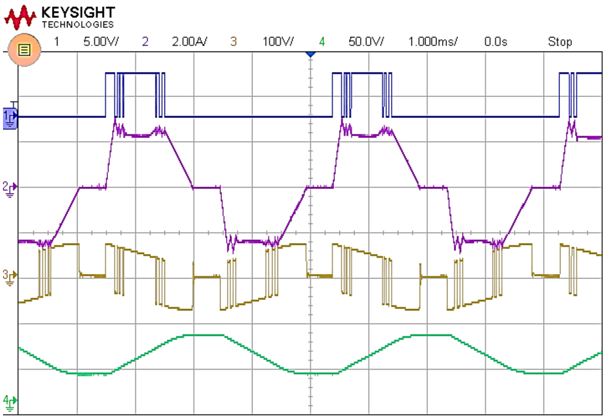

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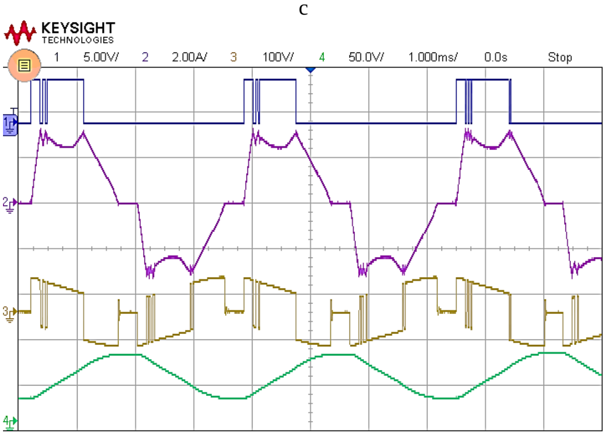

d

Fig. 8 Two phase SRM drive waveforms at different speeds channel 4, phase voltage associated to the phase 2 is being displayed.

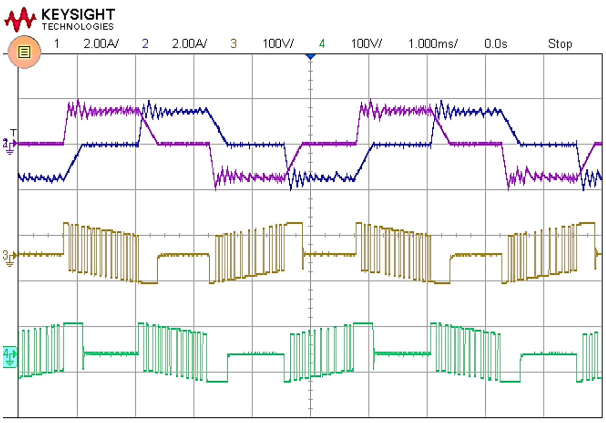

Fig. 9. Experimental results of the 2 phase half bridge based converter. Phase currents and voltages applied to an 4/2 SRM

In this section the possibility of using a modified half bridge-based converter topology, derived from conventional VSI (used for driving of 3 phase PMSMs) have been investigated at both simulation and experimental level. An advantage of employing such a topology is represented by the possibility of using massively produced three-phase full or half bridge packages, instead of conventional converter for SRM, which does not have a standardized converter package. Moreover, if discrete components are used, the conventional converter for SRM contains 2 more discrete diodes for each phase, which have a closed price to that of transistors, especially where high current capability is needed. By using the proposed converter, the elimination of the discrete diodes is accomplished, leading to price savings of semiconductors. However, the phase capacitor of the proposed topology is needed to be discussed, since it can affect the total cost of the converter. Considering that the price of the capacitor is directly proportional with its capacitance, a low value capacitance is required for good price balance. Furthermore the technology of the capacitor (polarized or non-polarized) can be also taken into discussion, since the polarized electrolytic capacitors can store higher energy, but with disadvantage of lower life span, while the un-polarized, have a lower energy capacity, but much higher reliability. With regards to the possibility of using non-polarized capacitor, the applications suitable for such a drive are in the low power range and high speed.

4. CONCLUSIONS

From the above presented results, one can conclude that the present converter topology has limitations, one being the fact that is not allowing the utilization at the maximum of DC bus voltage, which for automotive industry (where low dc bus voltage is available) can be a determining factor not to continue with the investigation of it. However, due to its advantages (highlighted in this work) it can be stated that there are some applications especially for high speed and low torque, such as electrically driven superchargers, high-speed hand-dryers or vacuum cleaners in which this topology can be used successfully.

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